ATTORNEY DOCKET NO. 321547US **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Simon Knowles
Serial No.:	10/813,615
Filed:	March 31, 2004
For:	APPARATUS AND METHOD FOR ASYMMETRIC DUAL PATH PROCESSING
Group No.:	2183
Examiner:	Robert E. Fennema Confirmation No: 3818

Mail Stop Appeal Brief-Patents

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/Jana R. Williford/
(Signature of the person signing the certificate)

Sir:

APPELLANT'S REPLY BRIEF UNDER 37 C.F.R. §41.41

In response to the Examiners Answer mailed July 7, 2010, the Appellant submits this Reply Brief in accordance with 37 C.F.R. §41.41.

I. Reply to Examiner's Answer

Hull Fails to Teach Control Instructions with a Bit Width that is a Control Bit Width

Regarding Claim 1, the Examiner suggests that Hull inherently discloses control instructions having a **control** bit width. (*See* page 4 of the Examiner's Answer.) The Appellant understands that it is inherent that all instructions have a bit width, but the Appellant disagrees that it is inherent that all instructions have a bit width that relates to the type of instruction. For example, Claim 1 includes: (1) control instructions having a bit width that is a "control bit width" and (2) data processing instruction having a bit width that is a "data processing bit width" which is "wider than the control bit width" of the control instructions.

In contrast, Hull teaches that all instructions have the same bit width. Therefore, if the control instructions of Hull have a bit width that is a **control** bit width as asserted by the Examiner, then, according to that interpretation, the data processing instructions of Hull would also have a bit width that is a **control** bit width. As noted above, this is clearly different than the control instructions and the data processing instructions of Claim 1 that have two different bit widths, respectively, a control bit width and a data processing bit width. Accordingly, for at least these reasons, the Appellant respectfully requests reversal of the Examiner's rejection and issuance of Claim 1 and the remaining pending claims.

The Combination of Hull and Hennessy is Improper and Fails to Teach Data Processing Instructions with a Bit Width that is a Data Processing Bit Width

The Examiner does acknowledge that Hull does not disclose the data processing instruction having a **data processing** bit width wider than the control bit width but suggests this would be

obvious in view of Hennessy which discusses a variable length architecture. (*See* pages 6-7 of the Examiner's Answer.) Hennessy also discusses BISC encoding, and gives a balanced and explanatory view concerning the advantage and disadvantages of each type of encoding. The Appellant notes as an example, page 130, Summary: Encoding the Instruction Set in which Hennessy states: "given the choice, the architect more interested in code size and performance will pick variable encoding, and the one more interested in performance than code size will pick fixed encoding." Hull wishes to retain the performance advantages of fixed encoding, while attempting to improve the instruction encoding efficiency of a BISC machine. Faced with the disclosures of Hull and Hennessy, a skilled person would not be motivated to attempt to adapt the disclosures of Hull to a variable length encoding machine, because that would sacrifice performance. Furthermore, the modifications that would be required to Hull are extensive and would involve a complete redesign of the machine in a manner which is clearly not disclosed to one of ordinary skill.

Hull states that in his invention "instructions are grouped together into 128-bit sized and aligned containers called bundles." (*See* column 2, lines 22-24.) If the instructions were of variable length, Hull could not use his bundles in the same way – he would have to reconsider entirely how the instructions were fetched from memory and would have to deal with how to align the instructions and how to identify their length. If the bundle concept of Hull cannot be used, it is difficult to see how the templates of Hull could be applied, because the templates depend on predefined slot positions which can accommodate instructions of the same length. As Hull states "(i)n other words, the template field specifies the mapping of instruction slots to execution unit types." (*See* column 3, lines 65-66.)

If the instructions of Hull were of varying length, this instruction slot concept could not be utilized. Note that Hennessy does not disclose the concept of control instructions having a control bit width and data processing instructions having a data processing bit width. Hennessy discloses that in a variable encoding machine, there can be a large number of different lengths of instructions "the length of 80 x 86 instructions varies between 1 and 17 bits." (*See* page 128, last section.)

The Examiner has identified a single example in Hennessy where one particular control instruction has a smaller length than two other data processing instructions, but this does not disclose the concept of control instructions having a width that is a control bit width and data processing instructions having a longer width that is a data processing bit width. On the contrary, Hennessy clearly discloses at least one control instruction (CALLF) which is longer than a data processing instruction (ADD). (*See* page D13 of Hennessy.) The Examiner has merely selected one particular example, which appears to have been selected based on hindsight using the claim language. There is nothing in Hennessy to suggest to a skilled person that there is anything particularly meaningful or important about the fact that one control instruction has a shorter length than some data processing instructions. In the full instruction set of Hennessy, the reverse must also be true.

Still further, the combination of Hull and Hennessy does not disclose to a skilled person how to accommodate variable length instructions in packets of a fixed size. In Hull, the instruction bundles can be of a fixed size because the instruction lengths are the same. In Hennessy, in a variable encoding system, the concept of packets does not arise.

Accordingly, Hennessy fails to cure the above noted deficiency of Hull and, even if the Hennessy did, the combination of Hennessy and Hull is improper. As such, Appellant respectfully

requests reversal of the Examiner's rejection and issuance of Claim 1 and the remaining pending claims.

Hull Fails to Teach A Control Processing Channel Including a Plurality of Functional Units

The Examiner also suggests that Hull discloses a control processing channel "comprising a plurality of functional units" as recited in Claim 1. (*See* pages 4-5 of the Examiner's Answer.) Hull, however, appears to disclose a single execution unit, a branch execution unit, for performing control operations. A single branch execution unit is not by itself sufficient to constitute a control processing channel comprising a **plurality** of functional units as recited in Claim 1.

The Examiner asserts that an execution unit of Hull or a group thereof discloses a processing channel. (*See* page 17, point 19, and the table on page 22, point 28.) As noted by the Examiner on page 19 of the Examiner's Answer, Hull does not disclose multiple branch execution units. (*See* point 23.) Even assuming the table on page 22 to be true for the sake of argument, a single execution unit capable of performing control operations, purportedly the branch execution unit of Hull, does not disclose a control processing channel with a **plurality** of functional units. Furthermore, the table suggests Hull has a processing channel with execution units. This differs from the architecture of Claim 1 that has two channels, a control processing channel and a data processing channel, wherein each of the different channels has a plurality of functional units and each of the different channels has a register file with different bit widths. Accordingly, for at least these reasons, the Appellant respectfully requests reversal of the Examiner's rejection and issuance of Claim 1 and the remaining pending claims.

Hull Fails to Teach A Decode Unit as Claimed

The Examiner suggests that Hull discloses wherein the decode unit...is configured to decode identification bits of each instruction **packet** to determine which **type** (1 or 2) of instruction packet is being decoded. (*See* page 5 of the Examiner's Answer. Emphasis added.) In Hull, however, packets are not understood by a decoder to fall into either type 1 or type 2. According to the Examiner's analysis, template E is an example of a bundle which includes at least one data processing instruction. Using this analysis of the Examiner, templates 0, 1, 2, 4, 5, 6, 7, 8, 9, and C would also be of type (ii) in accordance with the present invention. The selection of template E is an arbitrary selection by the Examiner with the claim language in mind – it is not singled out in Hull as having any particular or special quality for a skilled person.

For this reason, Hull fails to teach "wherein the decode unit causes instructions of type (ii) packets ... to be executed simultaneously on the data processing channel" as suggested by the Examiner. (*See* page 6 of the Examiner's Answer.) In Hull, only some bundles which would form within the category of having at least one data processing instruction include instructions which are executed simultaneously. Other bundles which include at least one data processing instruction in Hull do not include instructions which are executed simultaneously. This can be because of group boundaries which separate an instruction of one group from an instruction of another group within the same bundle (*see*, for example, column 4, lines 1 to 10). In this case, the instructions are executed in sequence. (*See* column 4, line 61.)

Also regarding Claim 1, the Examiner suggests that Hull discloses wherein the decode unit causes instructions of type 1 instruction packets to be executed sequentially on the control processing channel. (*See* page 5 of the Examiner's Answer referring to column 4, lines 61-62 of Hull). This passage in Hull refers to all bundles and not specifically only to template B which includes three instructions designated for branch units. This particular selection can only be made with hindsight with the claim language in mind – there is nothing to suggest to a skilled person that this passage in Hull reads only onto template B and not onto the other templates. In fact, it clearly does read onto all bundles as one skilled in the art would understand.

Moreover, Hull is silent as to how the bundle of template B will be executed. It is not shown to include stop bits to denote separation between slots (as in double line 43) and so it appears as though these instructions are intended to be executed simultaneously. Hull does not disclose that template B would be handled by executing the instructions in execution order, because that would require the existence of a stop bit in the template, which is not illustrated in Hull.

In section 10 of the Examiner's Answer, the Examiner appears to be reading **packet** onto **bundle** in Hull. (*See* page 17, point 19 and the table on page 22, point 28.) However, the determination as to which instructions are executed simultaneously is controlled by instruction groups in Hull, and not by their location in a particular bundle. Thus, the concept of type 1 or type 2 instruction packets which are handled differently by a decode unit is not disclosed in Hull.

Accordingly, for at least these reasons, Hull does not disclose each of the limitations of a decode unit as recited in Claim 1 and as relied on by the Examiner. The Appellant respectfully requests reversal of the Examiner's rejection and issuance of Claim 1 and the remaining pending claims.

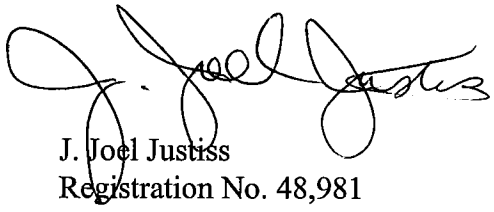
Due to the above-described deficiencies, the rejection of pending independent Claim 1 does not provide a *prima facie* case of obviousness. The Appellant also respectfully requests that the above applicable arguments be applied to independent Claims 18 and 21. Accordingly, the Appellant respectfully requests the Appeal Board to reverse the rejection of the Examiner and allow issuance of Claims 1, 18 and 21 and Claims dependent thereon.

II. Conclusion

For the reasons set forth above, the Claims on appeal are patentably nonobvious over the applied references. Accordingly, the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiners Final Rejection of all of the Appellants pending claims.

Respectfully submitted,

HITT GAINES, P.C.



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